AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to FIG. 1. This sheet replaces the original sheet containing FIG. 1. FIG. 1 has been amended with the legend "*PRIOR ART*."

Attachment: Replacement Sheet

REMARKS

Claims 1-12 are pending. Claims 1-11 have been cancelled. Claims 13-19 have been added. Claim 12 has been amended.

A telephonic interview was held on August 12, 2009 between attorney for Applicants Todd Li and Examiner Vongsavanh Sengdara and Primary Examiner Minh-Loan Tran. Todd Li explained that FIG. 1 illustrates prior art, while FIG. 6 illustrates an embodiment according to the invention. Agreement was reached that Applicants will amend FIG. 1 to indicate that it is prior art, and the claims will be amended to more clearly describe the invention as in the embodiment illustrated in FIG. 6.

Accordingly, a replacement sheet for FIG. 1 is hereby attached, wherein the legend "*PRIOR ART*" has been added to FIG. 1. Support is provided in paragraph [0020] which states that the "structure shown in Figure 6 is different than that shown in Figure 1 in that, in the structure shown in Figure 6, the emitter contact 124 is positioned within the wiring layer 120 instead of below the wiring layer 120 (as in the structure shown in Figure 1)." In addition, as stated in paragraph [0021], Figures 2-5 illustrate processing steps leading to FIG. 6. The specification points out that "[c]onventional processes reduce the raw height of the passivating film 112 down to the level 202." (see FIG. 2) Note that the level 202 (in FIG. 2) is similar to the level of the top surface of the passivation layer 112 in FIG. 1. Paragraph [0021] continues to state that "[h]owever, as shown in Figure 3, the invention reduces the height of the passivating layer 112 down to the level indicated by arrow 300 which is approximately equal to the top of the tallest device 302 (which in this example, is the top of the vertical bipolar transistor 118)." Applicants submit that FIG. 1 was intended to illustrate prior art, and thus no new matter has been added.

New independent claim 13 has been added to more clearly describe the invention in the embodiment as illustrated in FIG. 6. In particular, claim 13 recites "said passivating layer has a top surface substantially coplanar with said uppermost surface of said first type device." Support is provided at paragraph [0021]. Claim 13 also recites "a wiring layer above said passivating layer comprising a first device contact embedded therein that is in electrical contact with said uppermost surface of said first type device."

Support is provided in FIG. 6, paragraphs [0023] and paragraph [0027]. No new matter has been added.

Claim 12 has been amended to clarify that the method for forming the structure in claim 13 comprises forming said first device contact embedded within said insulating layer of said wiring layer using a dedicated photolithographic mask. Support is provided in paragraph [0023]. No new matter has been added.

Claims 12 and 14 recite said top surface of said passivating layer has a height within approximately 50 nm of the uppermost surface of said first type device. Support is provided at paragraph [0021]. No new matter has been added.

New claim 15 recites said first type device is a bipolar transistor. Support is provided throughout, e.g. paragraph [0021] (e.g. bipolar transistor 118). Claim 16 recites said first device contact is an emitter contact. Support is provided, for example, at paragraphs [0020] and [0023] (e.g. emitter contact 124). Claim 17 recites the emitter contact comprises a different material than said conductive wire feature. Support is provided at paragraph [0024]. Claim 18 recites said emitter contact comprises a material that is compatible with a chemical mechanical polishing process used on said conductive wire features. Support is provided at paragraph [0024]. Claim 19 recites said second type device is a CMOS transistor. Support is provided throughout the specification, for example, at paragraph [0026]. No new matter has been added.

Applicants respectfully request reconsideration of the objections and rejections in the Office Action dated May 29, 2009, based upon the following.

The drawings were objected to under 37 CFR 1.83(a), as not enumerating every feature of the invention specified in claims 1-8. Claims 1-8 have been cancelled, rendering those objections moot. Applicants respectfully request that these objections be withdrawn.

Referring to FIG. 1 and FIG. 6, the Examiner interpreted the claimed invention to mean the CE is a part of the NPN transistor and therefore the NPN device as interpreted is in a direct contact with the wiring layer. Applicants have amended FIG. 1 and hereby submit a replacement sheet for FIG. 1 to clarify that FIG. 1 is prior art. Applicants respectfully request that the objection to the drawings be reconsidered and withdrawn.

With respect to the CE and NPN transistor, Applicants respectfully disagree with the interpretation that the CE (emitter contact 124) is a part of the NPN transistor (bipolar transistor 118). For example, in paragraph [0021], the specification recites "as shown in Figure 3, the invention reduces the height of the passivating layer 112 down to the level indicated by arrow 300 which is approximately equal to the top of the tallest device 302 (which, in this example, is the top of the vertical bipolar transistor 118)." Thus the specification clearly identifies the top of the bipolar transistor 118 as surface 302 and does not include the emitter contact 124. The formation of the emitter contact 124, in accordance with the invention, is subsequently described in paragraph [0023] with reference to FIG. 4. Specifically, a dedicated photolithographic mask is used to pattern openings for the emitter contact 124 in the wiring layer 120. Also, in paragraph [0028] with reference to FIG. 7, the invention removes a portion of the passivating layer down to the top of the vertical bipolar transistors, and then the invention can form emitter contacts above the bipolar transistors. In view of the above, Applicants submit that the emitter contact (124) should be interpreted as a separate feature from the bipolar transistor (118).

Claims 1-11 and the specification were objected to because of informalities in the claimed subject matter. Similarly, claims 1-11 were rejected under 35 U.S.C. 112, second paragraph, as being allegedly indefinite. Claims 1-11 were cancelled, rendering those rejections moot, and Applicants request that those objections be withdrawn.

Claims 1, 2, 6, 7, 9, 10 and 12 were rejected under 35 U.S.C. 102(b) as being anticipated by Ohnishi et al. (6399993) (hereinafter "Ohnishi"). Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi. Claims 3, 4, 5 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi in view of Mori (2004/0021222).

As understood, Ohnishi discloses a bipolar transistor, including a base extended electrodes 22 and an emitter extended electrode 21. (col. 6, lines 19-37, with reference to FIG. 1) The interconnects 32, 33 and 34 and the titanium silicide layer 27, formed on these members, are connected together via contacts 30 passing through the interlevel dielectric film 29. (col. 6, lines 46-51, emphasis added). However, Ohnishi fails to disclose, teach or suggest a passivating layer positioned above said substrate and between said first and second type devices, wherein said passivating layer has a top surface

substantially coplanar with said uppermost surface of said first type device, and a wiring layer above said passivating layer comprising a first device contact embedded therein that is in electrical contact with said uppermost surface of said first type device. Thus, in Applicants' invention, the uppermost surface of the first type device (e.g. a bipolar transistor) is substantially coplanar with the top surface of the passivating layer and the first device contact (e.g. the emitter contact) is embedded in the wiring layer above the passivating layer (e.g. BPSG). Rather, in Ohnishi, the contacts 30 to the bipolar transistor pass through the ILD film.

As understood Mori discloses a semiconductor memory device including an interconnect stack. However, Mori fails to overcome the deficiencies of Ohnishi, and in particular fails to disclose, teach or suggest a passivating layer positioned above said substrate and between said first and second type devices, wherein said passivating layer has a top surface substantially coplanar with said uppermost surface of said first type device, and a wiring layer above said passivating layer comprising a first device contact embedded therein that is in electrical contact with said uppermost surface of said first type device.

For at least the reasons discussed above, Applicants respectfully submit that claim 13 is patentable over the prior art of record, and the dependent claims 12, and 14-19 are similarly patentable, and respectfully request that the rejections be reconsidered and withdrawn.

CONCLUSION

In view of the foregoing, Applicants submit that claims 13, 12, 14-19 are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time. The Commissioner is authorized to charge any additional fees due or credit overpayments to Deposit Account No. 09-0458.

Correspondence for this case should continue to be sent to:

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The undersigned may be reached at the address and phone number below.

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